QP Code: 9028QP

Seat No.	

Total No. of Pages: 3

Winter Examination Oct/Nov 2023

Subject Name: Bachelor of Engineering_67541_83856_83990 _ Advanced Computer Architecture_29.11.2023_10.30 AM To 01.00 PM

Subject Code: 83856

Day and Date: - Wednesday, 29-11-2023 **Total Marks: 70**

Time: - 10:30 am to 01:00 pm

Instructions.:

1) All questions are compulsory
2) Figures to the right indicate full marks
3) Assume suitable data wherever necessary and mention it boldly

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Q.1. **Q.1 Solve MCQs. (1 Marks Each)** **[14]**

1. Which of the following equation is correct?
1. Module availability = MTTF/ (MTTF + MTTR)
2. Module availability = MTBF/ (MTTF + MTTR)
3. Module availability = MTBF/ (MTTF - MTTR)
4. Module availability = MTTF/ (MTTF - MTTR)

2. In the S access memory organization, total time required to access k consecutive words in sequence starting in module i with a memory access time Ta and a latch delay of τ if i+k<=M
1. τ + kTa
2. τ + (k-1)Ta
3. Ta + (k-1)τ
4. Ta + kτ

3. Increase in volume
1. decrease the cost
2. decreases the learning curve
3. both (A) and (B)
4. None of the above

4. In SIMD computer, which of the following scheme is used to partitions the set of PEs into enabled and disable sets?
1. Routing scheme
2. Broadcasting
3. Network topology
4. Masking scheme

5. In ideal case, the maximum throughput that can be achieved with linear pipeline is
1. 1/τ
2. f
3. both (a) and (b)
4. k

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6. Ideally, a linear pipeline with k stages can process n tasks in_____ [14]
clock periods
1. k-(n+1)
2. k*(n-1)
3. k+(n+1)
4. k+(n-1)
7. In _____ , extra bits are kept in the cache to predict the way, or block within the set of the next cache access.
1. Set prediction
2. Cache prediction
3. Way prediction
4. None of the above
8. Which type of cache miss occur even if you had an infinite sized cache?
1. Compulsory
2. Capacity
3. Conflict
4. None of the above
9. Which technique is used to tackle the problem where the vector is longer than the maximum length?
1. chaining
2. stride
3. data mining
4. strip mining
10. The primary mechanism for supporting sparse matrices is_____using index vectors.
1. Masking operation
2. gather-scatter operations
3. stride operations
4. chaining operation
11. In GPU computational structure, _____ is assigned to the multithreaded SIMD Processor.
1. Grid
2. Thread Blocks
3. Threads
4. All of the above
12. Thread level parallelism is utilized by the following software model
1. Parallel processing
2. Request level parallelism
3. Multiprogramming
4. All the above

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13. A memory system is coherent if it
1. Preserve the program order
2. Preserve coherent view of memory
3. Ensures write serialization
4. All the above
14. In _____ cache coherence protocol, every cache that has a copy of the data from a block of physical memory could track the sharing status of the block.
1. Directory based
2. Snooping
3. Consistency
4. None of the above

Q.2. **Q2) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain the functional structure of SIMD array processor.
2. Define the two states of service with respect to an SLA. Explainthe two main measures of dependability.
3. Explain Handler's classification of pipeline processor according to levels of processing.

Q.3. **Q3) Solve any two of the following question (7 Marks Each)** **[14]**
1. Draw and explain S-access memory organization.
2. List and explain six basic cache optimizations in short.
3. Explain the use of nonblocking caches to increase the cache bandwidth.

Q.4. **Q4) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain the architecture of a typical vector processor with multiple functional pipes with neat diagram.
2. What is Vector Operand? Explain the classification of vector instructions into four primitive types with example.
3. Explain the components of Processing Element (PE) in SIMD computer.

Q.5. **Q5) Solve any two of the following question (7 Marks Each)** **[14]**
1. Explain NVIDIA GPU Computational Structure.
2. Explain the basic structure of a centralized shared-memory multiprocessor based on a multicore chip.
3. Explain directory based cache coherence protocol.