SP - 104

Total No. of Pages : 3

Seat No.	

T.Y. B.Tech. (Electronics and Telecommunication Engineering)
(Part - III) (Semester - V) Examination, December - 2023
PCC-ETC503 : DIGITAL AND VLSI DESIGN
Sub. Code : 80809

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Day and Date : Monday, 4 - 12 - 2023 **Total Marks : 70**

Time : 10.30 a.m. to 1.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Use suitable assumptions if required.**
3) **Draw necessary figures on right side of answer sheet.**

Q1) All questions are compulsory. **[7×2=14]**

a) Which of the following describes the structure of VHDL code correctly?
   i) Library Declaration; Entity Declaration; Architecture Declaration; Configurations
   ii) Entity Declaration; Configuration; Library Declaration; Architecture Declaration
   iii) Configuration; Library Declaration; Entity Declaration; Architecture Declaration
   iv) Library Declaration; Configuration; Entity Declaration; Architecture Declaration

b) One can't use more than one library in the VHDL code.
   i) True
   ii) False

c) Which of the following sequential circuit doesn't need a clock signal?
   i) Flip flop
   ii) Asynchronous counter
   iii) Shift register
   iv) Latch

d) Shift registers comprise of which flip-flops?
   i) D flip-flops
   ii) SR flip-flops
   iii) JK flip-flops
   iv) T flip-flops

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P.T.O.

e) Which of the following is used at the end of a statement?

i) ; (Semicolon)

ii) – (double hyphen)

iii) _ (underscore)

iv) No sign is used at the end of statement

f) What is the difference between SIGNAL and VARIABLE?

i) The value of SIGNAL never varies whereas VARIABLE can change its value

ii) SIGNAL can be used for input or output whereas VARIABLE acts as intermediate signals

iii) SIGNAL depends upon VARIABLE for various operations

iv) SIGNAL is global and VARIABLE is local to the process in which it is declared

g) The FPGA refers to

i) First programmable Gate Array

ii) Field Programmable Gate Array

iii) First Program Gate Array

iv) Field Program Gate Array

Q2) Solve any two **[2×7=14]**

a) Find out by using K-Map Minimization technique,

F(A,B,C,D) = Σm(0,5,8,9,10,l 1,14,15).

b) Write a VHDL program for Half Adder using if statement?

c) What is the difference between VHDL and Verilog?

Q3) Solve any two **[2×7=14]**

a) Write a VHDL program for 4 bit Parity bit generator.

b) Write VHDL program for 3:8 Decoder with enable pin.

c) Write VHDL program for 1:4 De-Multiplexer

Q4) Solve any two **[2×7=14]**

a) Write a VHDL program for JK Flip-flop.

b) Write Short note on DRAM/SRAM

c) Explain 1010 non overlapping sequence detector.

Q5) Solve any Two **[2×7=14]**

a) Write a VHDL code for 4 bit up and down Counter.

b) Write a VHDL code for PIPO Shift register

c) Explain in detail FPGA.

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