Seat No.

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MAR_APR 2025 SUMMER EXAMINATION

11731 Bachelor of Technology (NEP-2.0)

Sub. Name: Digital and VLSI Design

Sub. Code: 45694/80809/81066

Day and Date: MAY ,08-05-2025 **Total Marks: 70**

Time: 02:30 PM To 05:00 PM

Instructions: **1. All questions are compulsory**
2. Figures to the right indicate full marks

Q1) Solve following MCQ. **[14]**

i. The operator '&' is called the_____ operator.
A. Logical AND operator
B. Bitwise AND operator
C. Arithmetic addition operator
D. Concatenation operator

ii. Which of the following statement can't be used inside a process?
A. WAIT
B. IF ELSE
C. Variable declaration
D. PORT MAP

iii. Process is a _____ statement.
A. Concurrent
B. Sequential
C. Delay
D. Both concurrent and sequential

iv. How many flip flops are necessary to design a state machine with 25 states?
A. 2
B. 5
C. 25
D. 32

v. Refer to the VHDL code given below, which is the legal assignment statement?

```
SIGNAL x: STD_LOGIC;
SIGNAL y: STD_LOGIC_VECTOR (3 DOWNTO 0);
```

A. y <= (1 => '1', OTHERS => '0');
B. y := "0100";
C. y => "0100";
D. y => x;

vi. Which of the following is more volatile?

A. SRAM
B. DRAM
C. ROM
D. RAM

vii. PLA is used to implement _____

A. A complex sequential circuit
B. A simple sequential circuit
C. A complex combinational circuit
D. A simple combinational circuit

Q2) Attempt Any Two Questions **[14]**

a. Write a VHDL program for all Basic Gates. **[7]**

b. Write a VHDL program for Half Adder. **[7]**

c. Explain in detail Levels of abstraction in VHDL **[7]**

Q3) Attempt Any Two Questions **[14]**

a. Write a VHDL program for 4:1MUX **[7]**

b. Write VHDL program for barrel shifter. **[7]**

c. Write VHDL program 2 bit Comparator **[7]**

Q4) Attempt Any Two Questions **[14]**

a. Write a VHDL program for SIPO **[7]**

b. Write a VHDL program for T Latch **[7]**

c. Explain & convert SR to D flip flop **[7]**

Q5) Attempt Any Two Questions **[14]**

a. What is FSM? **[7]**

b. Write a VHDL code for 4 bit UP Counter. **[7]**

c. Explain in detail FPGA. **[7]**

End Of Question Paper

Important Note for Chief Exam Officer / SRPD Coordinator / Sr Supervisor/ Student -
This Question Paper may be distributed for following Subjects as common code.
सदरची प्रश्नपत्रिका खालील विषयांकरिता वितरित करता येईल.

1] (1154) B.Tech. CBCS (80809) Digital and VLSI Design Part 3 SEM 5
2] (101) Bachelor of Engineering (45694) VLSI Design Part 3 SEM 6
3] (101) Bachelor of Engineering (81066) Digital and VLSI Design Part 3 SEM 5