

Seat No. **OCT-NOV 2025 WINTER EXAMINATION****1154 B.Tech. CBCS****Sub. Name: Electroic Circuit Design - I****Sub. Code: 73247/77809****Day and Date: Friday ,05-12-2025****Total Marks: 70****Time: 02:30 PM To 05:00 PM**

Instructions: 1. All questions are compulsory
 2. Assume suitable data wherever necessary and mention it boldly
 3. Figures to the right indicate full marks

Special Inst.: Use component data sheet

- Q1) Solve all Questions [14]**
1. 1.1 An ideal power supply should have voltage regulation [2]
 A) More than 50% B) Between 10 to 15%
 C) Less than 1 % D) Almost 100%
 2. 1.2 A zener diode is destroyed if it..... [2]
 A) is forward biased B) is reverse biased
 C) Carries more than rated current D) none of the above
 3. 1.3 Consider a CE circuit, where trans-conductance is $50\text{m}\Omega^{-1}$, diffusion capacitance is 100 pF , transition capacitance is 3 pF . $I_B = 20\mu\text{A}$. Given base emitter dynamic resistance, $r_{be} = 1000\ \Omega$, input V_i is $20\sin(107t)$. What is the short circuit current gain [2]
 A) 30 B) 35
 C) 40 D) 100
 4. 1.4 If the value of $I_m=20\text{A}$ for FWR then the value of I_{dc} is _____ Amp. [2]
 A)10 B)6.36
 C)31.40 D)12.73
 5. 1.5. The h_{ie} parameter is called as _____ in CE arrangement with output shorted. [2]
 A)Voltage gain B)Current gain
 C)Input impedance D)None of the above
 6. c) Explain with diagram working of emitter follower [7]
 7. 1.7 Find the cut off frequency for an RC low pass filter of $R=200\Omega$ and $C=0.01\mu\text{F}$? [2]
 A)500KHz B)100Hz
 C)200KHz D)79.57KHz

- Q2) Solve any two** [14]
1. a]Design capacitor filter to supply $V_{dc} = 15V$, $I_{dc} = 80mA$ and $r = 0.05$ [7]
 2. b] Derive gain equation for High pass filter also design high pass filter with cut-off frequency 5 KHz and draw the frequency response [7]
 3. c]Explain with diagram working of emitter follower [7]
- Q3) Solve any two** [14]
1. a]Draw and explain negative clipper circuits [7]
 2. b]Design zener regulator with zener voltage $V_z = 12V$ to a load for which $I_L(max) = 150mA$, V_{in} varies between 20 to 25V [7]
 3. c]Derive the following terms for HWR: [7]
 - a. Dc voltage
 - b. Rms voltage
 - c. efficiency
 - d. ripple factor
 - e. form factor
 - f. TUF
 - g. PIV
- Q4) Solve any two** [14]
1. a]Derive A_v , A_i , R_i , R_o , A_{vg} , A_{ig} for general amplifier configuration using h-parameter model. [7]
 2. b]Design voltage divider bias circuit for following specifications $V_{cc} = 12V$, $I_c = 50mA$, $V_{ce} = 5V$, $h_{fe} = 50$, $V_{be} = 0.7V$ [7]
 3. c]Draw and explain high frequency model for transistor. Derive expression for f_B and f_T consider R_L . [7]
- Q5) Solve any two** [14]
1. a]Draw and explain hybrid equivalent circuit for CC configuration of transistor [7]
 2. b]Design single stage R-C coupled CE amplifier $V_{cc} = 12V$, $h_{fe} = 150$, $A_V = 60$, $h_{ie} = 2.2K\Omega$, frequency range 20Hz to 20 kHz, $S = 10$ [7]
 3. c]For CE amplifier has $h_{fe} = 100$, $h_{ie} = 2K\Omega$, $h_{oe} = 50 \times 10^{-6}$, $h_{re} = 2 \times 10^{-4}$, $R_c = 2K\Omega$, $R_L = 5.6K\Omega$, $R_1 = 10 K\Omega$, $R_2 = 4.7K\Omega$. Calculate A_v , A_i , Y_o . [7]

End Of Question Paper

Important Note for Chief Exam Officer / SRPD Coordinator / Sr Supervisor/ Student -

This Question Paper may be distributed for following Subjects as common code.

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1] (101) Bachelor of Engineering (77809) Electroic Circuit Design - I Part 2 SEM 3

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