ISSN: 2231-5063.

Implementation of FIR filter using VLSI.

[1]Mr.Sangram Patil,[2] Mr.Prithviraj Patil,[3]Mr.Indrajit Patil
[1,2,3]Students, Department of Electronics and Telecommunication
Bharati Vidyapeeth's College Of Engineering,
Kolhapur.
[1]patilsangram40@gmail.com[2]patilprithviraj1995@gmail.com[3]indrajitpatil494@gmail.com

[4]Prof.Sachin Jadhav
[4]Assistant Professor, Department of Electronics and Telecommunication
Bharati Vidyapeeth's College of Engineering,
Kolhapur.
[4]sachin30_2k6@redifmail.com

***Abstract*—A filter is used to pass a specific band of frequency. Depending on the response of the system, digital filters can be classified into Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Digital filters are widely used in many digital signal processing applications. Therefore digital filtering is one of the basic need of digital signal processing. Using windowing and sampling method FIR filter is designed. This paper introduces the definition and basic principle of FIR digital filters and design is based on VLSI.**

Keywords*— *FIR filters, hamming window, FPGA.

I. Introduction

Finite impulse response (FIR) filters are used in Digital Signal Processing applications. Accuracy in filter Designing is based on the Multiplication and accumulation of filter coefficients. Filters are digital filter whose response to the unit filter (Unit Sample Function) is finite in duration. This is in contrast to Infinite impulse response (IIR) filters whose response to unit impulse is infinite in duration FIR filter can be implemented using either recursive or non-recursive techniques, but usually non recursive technique are used.

FIR has following advantage over IIR Filter

- FIR filter is Finite IR filter and IIR filter is Infinite IR filter.
- FIR filters are non-recursive. That is, there is no feedback involved. Where as an IIR filter is recursive. There is feedback involved
- The impulse response of an FIR filter will eventually reach zero. The impulse response of an IIR filter may very well keep "ringing" ad-infinitum.
- IIR filters may be designed to accurately simulate "classical" analog filter responses where as FIR filters, in general, cannot do this.
- FIR filter has linear phase and easily control where as IIR filter has no particular phase and difficult to control
- FIR filter is stable and IIR filter is unstable
- FIR filter depend only on I/P where as IIR filter depend upon both I/P and O/p
- FIR filter consist of only zeroes and IIR filter consist of both poles and zeroes.

1.2 Structure of FIR filter

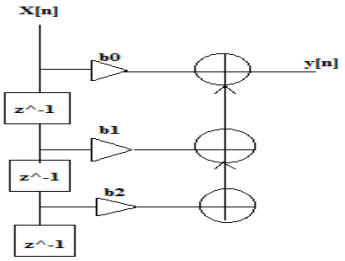

Fig.1 Structure of FIR filter

The goal of our project is to create a 4 tap FIR filter in VHDL. The goal is to get familiar with the tool chain and create the necessary components using Xilinx's Core Generator.

The equation to implement a FIR filter is given as:

$$y(n)=x(n)*h(n)=\sum_{k=0}^{l-1} f[k]x[n-1] \quad \text{---(1)}$$

II. Literature Review

In the literature review, different windows are used for the applications of Digital FIR filter design and spectral performance analysis.

In 2012SonikaAggarwalAashishGagnejaAmanPanghal worked on "Design of FIR Filter Using GA and its Comparison with Hamming window and Parks McClellan Optimization Techniques".Digital filter are widely used in the world of communication and computation. On the other hand to design a digital finite impulse response (FIR) filter that satisfying all the required conditions is a challenge. In this paper, design techniques of low pass FIR filters using Hamming window method, Optimal Parks McClellan method and Genetic Algorithm method are presented. The magnitude response, phase response, stability, and filter coefficients are demonstrated for different design techniques.

In 2015 Rashmi Patil, Dr.M.T.Kolte worked on "VLSI Implementation of FIR Filter for Discrete Wavelet Transform". Finite impulse response (FIR) filters are used in Digital Signal Processing applications. Accuracy in Filter Designing is based on the Multiplication and accumulation of filter coefficients. This describes an approach to the VLSI implementation of digital filter which is flexible and provides superior to traditional approaches, low power, and area efficient Discrete Wavelet Transform architecture.

III. Working Principle

FIR filter can be designed using frequency sampling and windowing method. But in windowing method, infinite impulse response of the prescribed filter is truncated by using a Window function. The main advantage of this design technique is that the impulse response coefficient can be obtained in closed form and can be determined very easily and quickly. The Window method is simple in operation, easy to understand and very convenient method for designing digital FIR filter. The most popular and widely used window functions are: Rectangular window, Hanning window, hamming window and Kaiser window.

IV. Implementation of FIR Filters

The implementation of an FIR requires three basic building blocks
– Multiplication
– Addition
– Signal delay

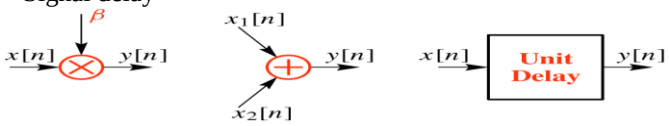

Fig.1 Building Blocks of multiplier, adder, delay.

Multiplier: $y[n]=\beta x[n]$

• In a DSP system the multiplier must be fast and must have sufficient precision (bit width; think logic circuits) to support the desired application
• A high quality filter will in general require more multiplications than one of lesser quality, so throughput suffers if the multiplier is not fast
– There are classes of filters that do not require multiplies
• FIR filters having 50 coefficients or more are not that uncommon

Adder: $y[n]=x_1[n]+x_2[n]$

• Signal addition is a very basic DSP function
• In an FIR filter additions are required in combination with multiplications, hence DSP microprocessors feature multiply- accumulate (MAC) units
• Adders generally operate with just two inputs at a time

Unit Delay: $y[n]=x[n-1]$

• The unit delay provides a one sample signal delay
• A sample value is stored in a memory slot for one sample clock cycle, and then made available as an input to the next processing stage
• An *M*-unit delay requires *M* memory cells (note each memory cell must store say *B*-bits) configured as a shift register (*B*-bits wide)

ISSN: 2231-5063.

V. DESIGN STEPS FOR FIR FILTERS VIA WINDOW METHOD

- Define filter specifications.
- Specify the window functions according to the filter specifications.
- Compute the filter order required for a given set of specifications.
- Compute the window function coefficients.
- Compute the ideal filter coefficients according to the filter order.
- Compute FIR filter coefficients according to the obtained window function and ideal filter coefficients.
- If the resulting filter has too wide or too narrow transition region, it is necessary to change the filter order by increasing or decreasing it according to needs, and after that steps 4, 5 and 6 are iterated as many times as needed.

VI. Results

Table 1.Summery of device utilization

Synthesis particilars	Utilization details	Utilization in %
Selected Device	3sd3400afg676-4	-
Number of Slices	14 out of 23872	0%
Number of Slice Flip Flops	16 out of 47744	0%
Number of 4 input LUTs	26 out of 47744	0%
Number of IOs:	25	-
Number of bonded IOBs	25 out of 469	5%
Number of GCLKs:	1 out of 24	4%
Number of DSP48s	2 out of 126	1%

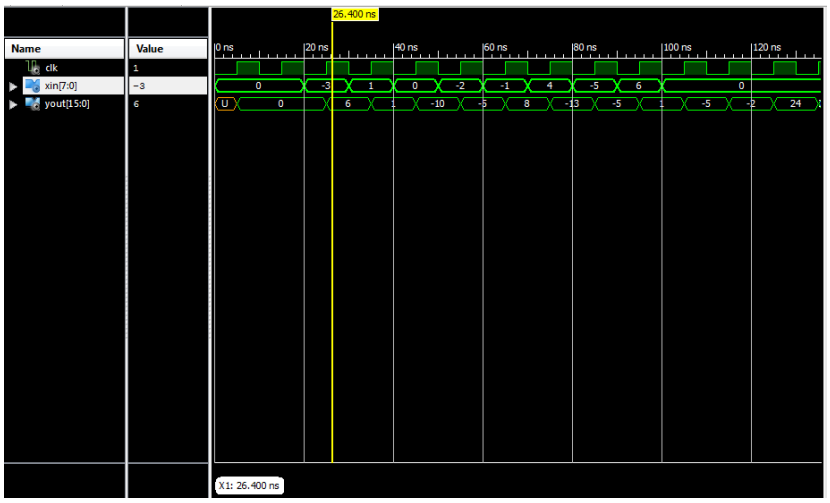

Fig.2 Simulation result

Table.2 output response of 4 tap FIR filter

H[n]	-2	-1	3	4	Y[out]
X[n]	-3	0	0	0	6
	1	-3	0	0	1
	0	1	-3	0	-10
	-2	0	1	-3	-5
	-1	-2	0	1	8
	4	-1	-2	0	-13
	-5	4	-1	-2	-5
	6	-5	4	-1	-2

VII. Application

1. Noise suppression
   (a) Imaging devices (medical, etc)
   (b) Biosignals (heart, brain)
   (c) Signals stored on analog media (tapes)
2. Enhancement of selected frequency ranges
   (a) Equalizers for audio systems (increasing the bass)
   (b) Edge enhancement in images
3. Removal or attenuation of selected frequencies
   (a) Removing the DC component of a signal
   (b) Removing interferences at a specific frequency
4. Bandwidth limiting
   (a) anti-aliasing filters for sampling
   (b) Ensuring that a transmitted signal occupies only its allotted frequency band.

VIII. Future Scope

In this project we are only simulate FIR filter, we can further implement on FPGA or CPLD Board according to requirement.

IX. Conclusion

This paper present implementation of 4 tap FIR filter using windowing technique. We Have found delay time 5.156ns to produce output response at frequency 193.949MHZ of FIR filter. It may be used to enhance speed of FIR filter response. After implementation we found that very less number of the devices utilized for synthesis and simulation.

Acknowledgment

I sincerely acknowledge the immense contribution of Er.S.B.Jadhav&Er.VeereshP.M(Assistant Professor, Department of Electronics and Telecommunication Engineering, Bharati Vidyapeeth's College of Engineering Kolhapur) for their guidance, encouragement and supervision during the period of this work.

References

1.Abdullah Mohamed Awad "Adaptive Window Method of FIR filter Design" IEEE conference on open system, 2010
2.ArojitRoychowdhury, "FIR Filter Design Techniques" 3.Electronic Systems Group, EE Dept, IIT Bombay.
J.G.Proakis and D.G.Manolakis, "Digital Signal Processing Principles, Algorithms and Applications" third edition Prentice-Hall, 2002.
4. Sanjit K. Mitra, "Digital Signal Processing: A computer-base approach", Tata McGraw-Hill, 2nd Ed, 2001.
5. Gennaro Evangelista, "Design of Optimum High Order Finite Word length Digital FIR Filters with Linear.
6.NurhanKaraboga, "Optimal Design of Minimum Phase digital FIR filter using genetic algorithm"
7. S. Salivahanan, A. Vallavaraj, C. Gnanaapriya, "Digital Signal Processing", Tata McGraw-Hill.